KU-BAND MONOLITHIC 7-WATT POWER AMPLIFIER USING AlGaAs/GaAs 0.25-μm T-GATE HETEROSTRUCTURE FET TECHNOLOGY

Danny T. Bryant, Keith Salzman, and Rick Hudgens

Texas Instruments Incorporated
Dallas, Texas 75265

ABSTRACT

Two advanced Ku-band MMIC power amplifiers have demonstrated state-of-the-art performance at upper Ku-band. One design delivers 7.2 watts CW (9.3 watts pulsed) at 25-percent power-added efficiency (PAE). The other design delivers 32-percent PAE at 2.7 watts CW.

INTRODUCTION

Ku-band solid-state phased-array radar and communication systems will require high performance MMICs to meet system performance and costs goals. Two Ku-band MMIC power amplifier designs were designed and fabricated using 0.25-μm T-gate technology on 100-μm HFET material. All RF, dc, and stability components are on-chip to reduce costs in high-volume applications. Both designs feature ground-signal RF probe pads to permit full characterization of each MMIC before chip separation to ensure high yields at higher level assembly.

MATERIAL STRUCTURE AND DEVICE FABRICATION

A cross-sectional view of the device and material structure for the HFET [1] is shown in Figure 1. The active GaAs layer, doped low to mid 10^{17} cm^{-3}, is separated from the gate junction by a mid to high 10^{16} cm^{-3} doped AlGaAs layer. A highly doped GaAs layer at the surface is used to improve ohmic contact resistance. The separation between the gate and active layer gives the device constant transconductance as a function of gate voltage. The superlatice buffer provides charge confinement that gives the device a sharp pinchoff characteristic and low output conductance. These material features are ideal for high-efficiency operation.

The device is fabricated using alloyed Au/Ge for ohmic contacts and boron ion implantation for device isolation. Selective reactive ion etching with CCl_4 [2] was used to put the first recess at the GaAs/AlGaAs interface.

The 0.25-μm T-shaped gate of the device improves the high frequency response over conventional FETs by reducing gate length and gate resistance. The Schottky barrier formed between the gate and the high-bandgap AlGaAs increases the breakdown voltage and makes the device suitable for high voltage operation.

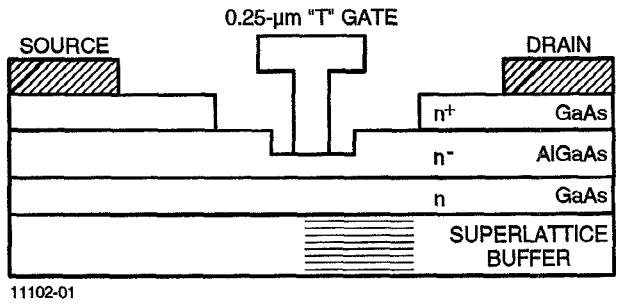

Figure 1. 0.25-μm T-Gate AlGaAs/GaAs Heterostructure FET

7-WATT MMIC DESIGN

The power level goal for the larger MMIC was 6 watts CW. Our anticipated output circuit loss was 1.2 dB and our previous 0.25-μm process power density was 0.5 W/mm. These numbers suggested an output FET of approximately 16 mm. To avoid 1-mm or larger FET cells the designer decided on a 16-cell output of 980 μm per cell (15.68 mm total). The FET cell was derived from the 840-μm serpentine structure used in TIs 2.5-watt ion-implant Ku-band MMIC [3]. This 840-μm cell uses 14 60 μm gates in a thermally efficient layout. The gates were lengthened to a still conservative 70-μm to achieve the 980-μm cell. Approximately 8 μm of extra width was inserted into the FET cell to achieve a via-to-via spacing of exactly 360 μm. The 360 is divisible by many numbers that would allow a good grid size for Sonnet EM (electromagnetic) simulation of the matching structures near the output FET. All major manifolds and junctions were optimized at 17 GHz for minimum loss [dB (g_{max})] using the Sonnet EM (Sonnet Software) program and LIBRA (EEsof). The grid sizes used was 5, 6, 10, and 15 μm. Although the MMIC required some on-chip tuning to optimize its performance [3][4] 17 GHz was always the frequency of best performance. The Sonnet EM optimization was primarily mitering right angles. The output circuit design uses load-line techniques [5] to correctly load the output FET. Binary combining is used to connect the 16 cells to the output bond

pad. Both input and output are designed to work with optimum-microstrip- interconnects [3][6]. Using Sonnet EM to miter the junctions reduced the output circuit loss from 2.1 dB (Sonnet/LIBRA prediction) to 1.2 dB (predicted). Both interstages use reactive matching. The second interstage is designed to load the center FET for best large-signal power delivery. The first interstage is designed for best small-signal gain flatness. The input circuit is designed for good input VSWR. The center FET is eight cells of 672 µm each for a total of 5,376 µm. Each 672-µm cell is a 12-finger serpentine structure using 56-µm gates for good Ku-band gain and reduced temperature operation. The eight cells are implemented as two four-cell FETs for even cooler operation. To physically drive the two four-cell center FETs from a common input feed point two spider FETs [7] are used as the first FET. The spider FETs allow a 90-degree signal flow with the gates going in the same direction as the serpentine FETs. Each spider FET is 1,200 µm (50 µm × 24) for a total of 2,400 µm first FET. The spider layout allows short gates and reduced temperature operation (compared to a conventional 1,200-µm cell). The total FET on this MMIC is 23,456 µm. The chip size is 6.2 × 6.5 mm (0.244 × 0.256 inch) (W×L). The 7-watt amplifier is shown in Figure 2.

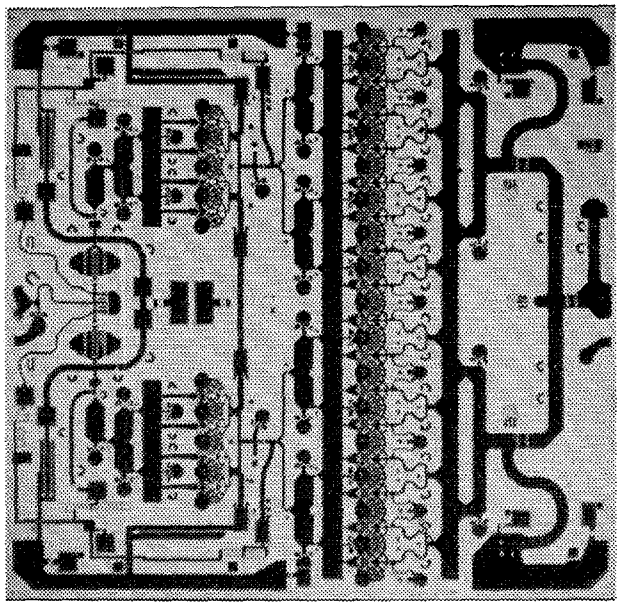

Figure 2. 7-Watt Ku-Band Power Amplifier (3266-56)

3-WATT MMIC DESIGN

The smaller MMIC is designed with T/R radar modules in mind. Two MMICs side by side power combined with Lange couplers are only 6.8 mm (0.268 inch) wide. The output FET uses eight cells of the 980-µm serpentine (7,840 µm). The same design philosophy was used on the smaller MMIC as the larger MMIC. The center FET is four cells of 720 µm each (2,880 µm). The first FET is two cells of 648 µm each (1,296 µm). The first and second FETs use conventional FET layout. This smaller MMIC also uses Sonnet EM analysis, is also RF probable, and also uses optimum-microstrip-interconnects. This device is the same area 19.4 mm^2) as TIs ion-implanted Ku-band 2.5-watt MMIC but delivers more power and more efficiency in a narrower design. The total FET on this MMIC is 12 mm. The chip size is 3.35 × 5.8 mm (0.132 × 0.229 inch) (W×L). The 32-percent efficient amplifier is shown in Figure 3.

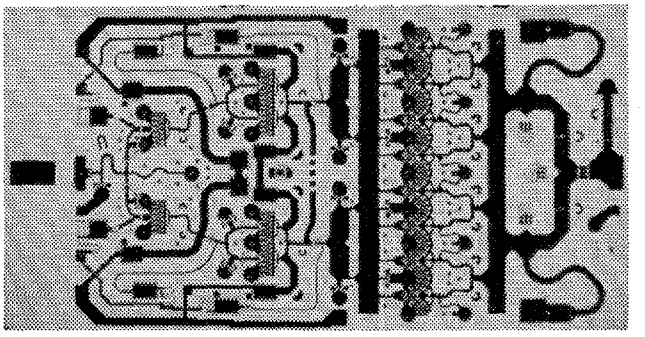

Figure 3. 3-Watt Ku-Band Power Amplifier (3266-55)

RF PERFORMANCE

All performance is after some on-chip tuning to optimize performance. Figure 4 compares the output power of the larger MMIC CW with 30-dBm input power and pulsed [(10 µs pulsewidth 100-µs period (10-percent duty cycle))] with 28-dBm input power. The drain voltage is 9 volts at

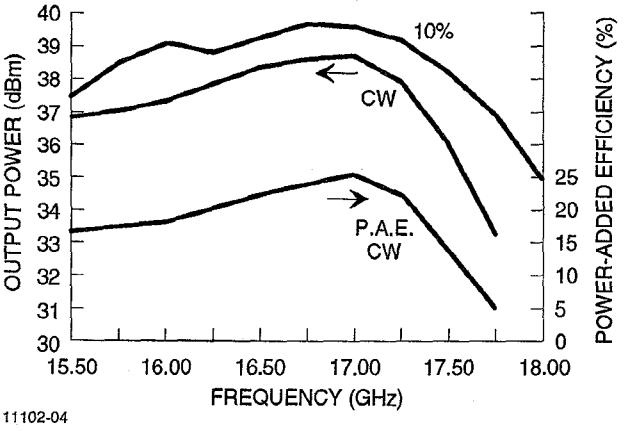

Figure 4. 7-Watt MMIC CW Efficiency and CW Versus Pulsed Output Power

room temperature. Note the 9.3 watts pulsed and 7.2 watts CW at 17 GHz with good performance from 15.5 to 17.5 GHz. CW efficiency is also shown in Figure 4. Note CW efficiencies of 20 to 25 percent from 16.3 to 17.3 GHz. Figure 5 shows small signal gain and input return loss. The CW room-temperature gain is 12 to 14 dB from 16 to 17.6 GHz with input return loss greater than 10 dB above 16.5 GHz. Figure 6 shows a balanced pair of the larger MMICs. The assembly is only 13 × 18 mm (0.5 × 0.7 inch). The 10-percent duty cycle performance is shown in Figure 7.

The drain voltage is 9 volts with an input power of 31 dBm. Note the 12 to 15.7 watts from 15.75 to 17.6 GHz with efficiencies of 20 to 25 percent. The smaller MMIC output power when biased for efficiency is shown in Figure 8. Note efficiencies of 26 to 32 percent CW with output powers of 2.3 to 2.8 watts from 16.5 to 17.6 GHz. The drain voltage is 9 volts at 25°C. The smaller MMIC output power when biased for power is shown in Figure 9. Note the 2.5 to 3.3 watts CW with efficiencies of 23 to 29 percent from 16 to 17.7 GHz. The drain voltage is 9 volts with 21-dBm input power at 25°C. Figure 10 shows small-signal gain and input

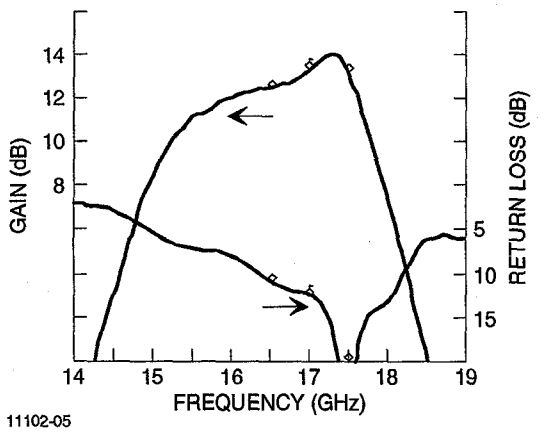

Figure 5. 7-Watt MMIC CW Gain and Input Return Loss

Figure 6. 15.7-Watt Ku-Band Power Amplifier Assembly (68-935)

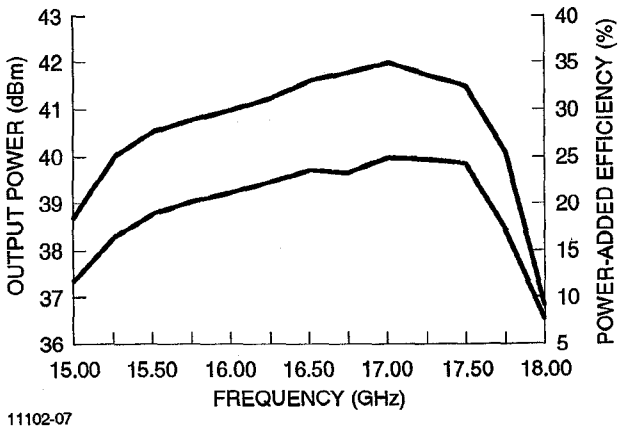

Figure 7. 15.7-Watt Balance Pair Performance

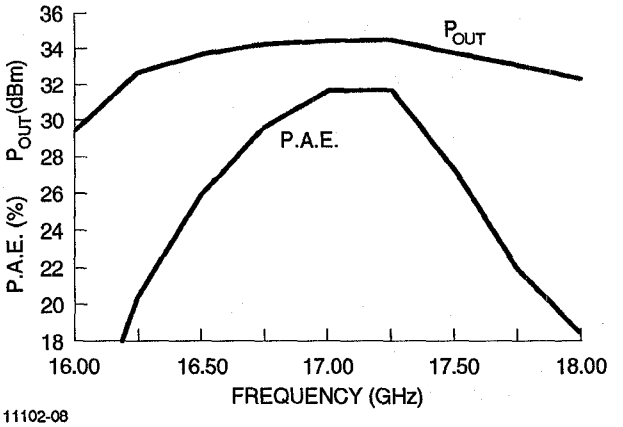

Figure 8. 3-Watt MMIC Performance, Biased for Efficiency

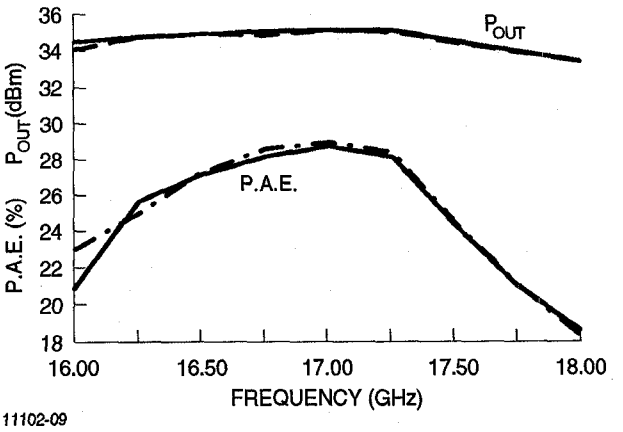

Figure 9. 3-Watt MMIC Performance, Biased for Power

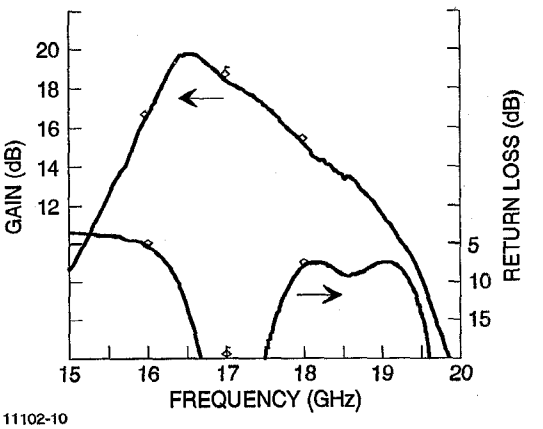

Figure 10. 3-Watt MMIC CW Gain and Input Return Loss

return loss for the smaller MMIC. Note the 16 to 20 dB of CW gain from 15.9 to 17.8 GHz and the input return loss exceeding 14 from 16.5 to 17.6 GHz.

CONCLUSION

Advances in materials and processing have allowed a 6-watt design to deliver 7.2 watts from one of two successful designs fabricated together. Electromagnetic simulator (Sonnet EM) analysis also contributed to design success of both circuits. A narrow 3-watt 30-percent efficient Ku-band MMIC is ready for phased-array radar T/R module applications. Power combining two of the 7-watt (9-watt pulsed) MMICs has delivered 15.7 watts (pulsed) in a small simple 13- × 18- mm assembly.

ACKNOWLEDGEMENTS

Thanks go out to Lou Nell Carroll, Bonnie Hilton, Faye Rangel, Marilyn (Youngblood) Stegemoller, Megan (Ryan) Frizzell, and the others who assisted in the assembly and tuning of the amplifiers.

REFERENCES

1. P. Saunier, et al, "A Heterostructure FET With 75.8 Percent Power Added Efficiency at 10 GHZ", 1992 IEEE MTT-S Digest, pp. 635-638.

2. B. Mercer, K. Salzman, and S. Singh, "A Highly Selective Plasma Gate Channel Recessing Technique for Fabrication of GaAs/AlGaAs heterostructure FETs", 1992 U.S. Conference on GaAs MANufacturing TECHnology Digest, pp. 45-47.

3. Danny T. Bryant,"Ku-Band Monolithic 2.5-Watt Power Amplifier for High Volume Applications", IEEE MTT-S 1991, pp 421-424.

4. David D. Heston and Randall E. Lehmann,"Monolithic Breadboard: Key to Radical MMIC Size Reduction", Microwave Journal, Vol. 33, No. 4, April 1990, pp 283-286.

5. S. C. Cripps,"A Theory for the Prediction of GaAs FET Load-Pull Power Contours", IEEE MTT-S 1983, pp 221-224.

6. Steve Nelson, Marilyn Youngblood (Stegemoller), Jeanne Pavio, Brad Larson, and Rick Kottman,"Optimum Microstrip Interconnects", IEEE MTT-S 1991, PP 1071-1074.

7. Austin Truitt, David Heston, and James Klein,"New Low Noise FET Structure", IEEE MTT-S 1990, pp 751-752.